REMARKS

Claims 1 and 3-15 are pending in this application. Claims 1, 4-6 and 13 are cancelled without prejudice or waiver. Claims 3, 7-9, 10-12 and 14-15 are amended and new claims 16-26 are added herein. Claims 7-9, as amended, are independent claims. The changes to the amended claims are shown in the Appendix hereto, as required by 37 C.F.R. §1.121, with deletions indicated by bracketing and additions indicated by underlining.

In the Action, the Examiner objects to claim 1 on the grounds that the phrase "plurality of semiconductors," in line 3, should be replaced by --plurality of semiconductor devices--. The limitations of claim 1 are incorporated into claims 7-9, as discussed below, and although claim 1 is cancelled herein, the correction suggested by the Examiner has nevertheless been made. The Examiner also objects that claim 6 is of improper dependent form for failing to further limit the subject matter of a previous claim. It is submitted that this objection is moot because of the cancellation herein of claim 6. Accordingly, it is respectfully requested that the Examiner's claim objections be withdrawn.

Claims 7-9 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner asserts that the use of the word "predetermined" in claims 7-9, reads on a nebulous mental step conducted prior to the manipulative steps of the claimed invention, hence rendering the present process claims unclear in meaning and scope. While it is not possible to specify a range of time because of the variability of the characteristics of different thermosetting resins, the Examiner's concerns have been addressed by replacing the phrase "a predetermined time" with --a period of time determined to be sufficient for said voids to be eliminated--. It is respectfully submitted that the new wording sets forth a definitive standard by which an appropriate time period for any given resin system can be readily determined.

The Examiner also rejects as unclear the use of the term "easy" in claims 7-9, use of the term "reduced" in claim 8, line 6, and use of the term "void removal temperature" in claim 9. All of these terms have been eliminated in a general rewrite of

the paragraphs beginning "wherein" at the end of each of claims 7-9, intended to make the meaning and scope of these claims more clear. In view of the changes made in claims 7-9, it is respectfully requested that their rejection by the Examiner under §112, second paragraph, be reconsidered and withdrawn.

Claims 1, 3, 4, 6 and 11-13 stand rejected under 35 USC §102(e) as being anticipated by Chakravorty, U.S. Patent No. 6,181,569. It is respectfully submitted that the rejection is moot with respect to claims 1, 4, 6 and 13 because of their cancellation herein. It is further submitted that claims 3, 11 and 12, which are amended herein to depend directly or indirectly from claim 7, patentably distinguish over the Chakravorty reference for at least the reasons discussed below in regard to claim 7.

Claims 1, 5 and 10 stand rejected under 35 USC §103(a) as being obvious over Gilleo et al., U.S. Publ. No. 20010003058, in combination with Chakravorty. It is respectfully submitted that the rejection is moot with respect to claims 1 and 5 because of their cancellation herein. It is further submitted that claim 10, which is amended herein to depend from claim 7, patentably distinguishes over the applied art combination for at least the reasons discussed below in regard to claim 7.

Claims 7-9, 14 and 15 stand rejected under 35 U.S.C. §103(a) as being obvious over Chakravorty, as applied by the Examiner to claims 1, 3, 4, 6, and 11-13. Except to the extent addressed by the amendments herein to the rejected claims, the rejection is respectfully traversed.

The Examiner's rejection of each of claims 7-9 begins with the premise that Chakravorty teaches the method of manufacturing semiconductor device originally recited in claim 1, and which is now incorporated in claims 7-9. The applicant disagrees. The manufacturing method, as claimed in the present application, recites "placing a sheet of encapsulating material containing a thermosetting resin having a curing temperature over said semiconductor wafer so as to cover said main surface," and "heating and curing said sheet encapsulating material by a heating apparatus to thereby form an encapsulating resin layer." Chakravorty discloses that encapsulation can be done by a number of established approaches such as transfer molding using epoxy resin based mold compounds, laminating with a dry film such as polyimide or other polymeric material, or coating from a liquid solution using techniques such as

extrusion, curtain, meniscus, or spin coating (see Chakravorty column 9, line 65, through column 10, line 3). The lamination process disclosed in Chakravorty involves laminating the dry film to the semiconductor wafer using an epoxy adhesive glue (see column 10, lines 29-30), and hence, is not equivalent to the process disclosed in the present application, where no adhesive is required. Moreover, Chakravorty fails to expressly disclose that the encapsulation material used is a thermosetting resin, as the rejected claims require.

Claims 7-9 each recite limitations that further distinguish over Chakravorty. For example, each of these claims require that the heating and curing step be done in such a manner that the heating of the sheet encapsulating material is at a heating temperature lower than the curing temperature of the sheet encapsulating material, at which the viscosity of the sheet encapsulating material is low and voids contained in the sheet encapsulating material can escape, and that the sheet encapsulating material be kept at the heating temperature for a period of time determined to be sufficient for the voids to be eliminated. It is respectfully submitted that neither Chakravorty nor Gilleo teach or suggest that the curing process includes maintaining the encapsulating material at a heating temperature less than the curing temperature for a period of time, during which the viscosity of the encapsulating material will be low and any voids in the encapsulating material will be able to escape.

The Examiner fails to point out anything in the references that discusses the problem of voids in the encapsulating material, or a process by which they may be eliminated. The Examiner's argument is simply that the heating step recited in claims 7 and 8 would be performed during the process of heating the resin to the curing temperature. The applicant disagrees and respectfully submits that it is not inherent in the processes disclosed in the prior art references to dwell at a temperature below the curing temperature for a period of time. On the contrary, without a clear reason to pause in the heating process, the reasonable course of action would be to raise the temperature as quickly as possible in order minimize process time.

With regard to the step of heating the encapsulating material at reduced pressure recited in claims 8 and 9, the Examiner takes official notice that it was known at the time of the applicant's invention to coat a semiconductor substrate having bump

electrodes with resin at a reduce pressure followed by raising the pressure to achieve uniform coating including reduction of voids. The Examiner provides no references, affidavit or other documentation in support of this finding. Similarly, the Examiner fails to provide support for the official notice taken, regarding claim 14, that the use of sheet encapsulating material containing a curing agent enclosed in a capsule to broken at a curing temperature was known prior to applicant's invention. Further, the Examiner fails entirely to address the features recited in claim 15.

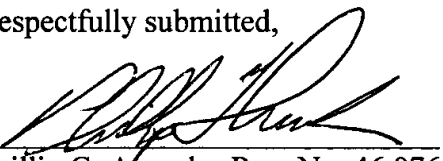
Accordingly, it is respectfully submitted that the Examiner has not met the burden of establishing a prima facie case of obviousness with regard to claims 7-9, 14 and 15, and that the rejection of these claims should be withdrawn.

As noted above, claims 7, 8 and 9 are amended herein to incorporate the limitations of canceled claim 1. Claims formerly depending from claim 1 have been amended to depend directly or indirectly from claim 7. New claims 16-26 reiterate the features to which dependent claims 3, 10-12 and 14-15 are directed, but depend from newly independent claims 8 and 9.

In summary, it is submitted that this application, as amended, is in condition for allowance. Such action, and the passing of this case to issue are respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



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APPENDIX

AMENDED CLAIMS

(With deletions in brackets and additions underlined)

3. (Twice Amended) The method as claimed in claim [1] 7, further comprising:

forming external terminals each having conductivity so as to be connected to said bumps respectively.

7. (Twice Amended) A [The] method [as claimed in claim 1,] of manufacturing semiconductor devices, comprising:

forming a plurality of semiconductor devices on a main surface of a semiconductor wafer, the plurality of semiconductor devices having a plurality of electrode pads for respectively connecting thereto;

forming a plurality of bumps on said main surface that are respectively connected to said electrode pads;

placing a sheet of encapsulating material containing a thermosetting resin having a curing temperature over said semiconductor wafer so as to cover said main surface;

heating and curing said sheet encapsulating material by a heating apparatus to thereby form an encapsulating resin layer;

polishing said encapsulating resin layer to expose portions of said plurality of bumps; and

dividing said semiconductor wafer into individual semiconductor device chips;

wherein said heating and curing are done in such a manner that the heating of said sheet encapsulating material is at a heating temperature lower than the curing temperature of said sheet encapsulating material, [and] at which the viscosity of said sheet encapsulating material is [kept] low and voids contained in said sheet encapsulating material can escape, and said sheet encapsulating material is kept at said heating temperature for a [predetermined] period of time determined to be sufficient for said [at a temperature at which] voids [contained in said sheet encapsulating material are easy] to be eliminated, and thereafter said sheet encapsulating material is increased in temperature to said curing temperature or higher.

8. (Twice Amended) A [The] method [as claimed in claim 1,] of manufacturing semiconductor devices, comprising:

forming a plurality of semiconductor devices on a main surface of a semiconductor wafer, the plurality of semiconductor devices having a plurality of electrode pads for respectively connecting thereto;

forming a plurality of bumps on said main surface that are respectively connected to said electrode pads;

placing a sheet of encapsulating material containing a thermosetting resin having a curing temperature over said semiconductor wafer so as to cover said main surface;

heating and curing said sheet encapsulating material by a heating apparatus to thereby form an encapsulating resin layer;

polishing said encapsulating resin layer to expose portions of said plurality of bumps; and

dividing said semiconductor wafer into individual semiconductor device chips;

wherein said heating and curing are done in such a manner that the heating of said sheet encapsulating material is at a heating temperature lower than the curing temperature of said sheet encapsulating material, [and] at which the viscosity of said sheet encapsulated material is [kept] low and voids contained in said sheet encapsulating material can escape, and said sheet encapsulating material is kept at said heating temperature and at a reduced pressure lower than atmospheric pressure for a [predetermined] period of time [at a reduced pressure at a temperature at which] determined to be sufficient for said voids [contained in said sheet encapsulating material is easy] to be eliminated, and thereafter said sheet encapsulating material is increased in temperature to said curing temperature or higher.

9. (Twice Amended) A [The] method [as claimed in claim 1,] of manufacturing semiconductor devices, comprising:

forming a plurality of semiconductor devices on a main surface of a semiconductor wafer, the plurality of semiconductor devices having a plurality of electrode pads for respectively connecting thereto;

forming a plurality of bumps on said main surface that are respectively connected to said electrode pads;

placing a sheet of encapsulating material containing a thermosetting resin having a curing temperature over said semiconductor wafer so as to cover said main surface;

heating and curing said sheet encapsulating material by a heating apparatus to thereby form an encapsulating resin layer;

polishing said encapsulating resin layer to expose portions of said plurality of bumps; and

dividing said semiconductor wafer into individual semiconductor device chips;

wherein said heating and curing are done in such a manner that the heating of said sheet encapsulated material is at a heating temperature lower than the curing temperature of said sheet encapsulating material, [and] at which the viscosity of said sheet encapsulating material is [kept] low and voids contained in said sheet encapsulating material can escape, and said sheet encapsulated material is kept for a first [predetermined] period of time under a first reduced pressure lower than atmospheric pressures at [a void removal] said heating temperature, [at which voids contained in said sheet encapsulating material are easy to be eliminated,] and thereafter repeatedly held plural times for a second [predetermined] period of time while being kept at [the void removal] said heating temperature at a second reduced pressure between the first reduced pressure and atmospheric pressure, the sheet encapsulating material being kept at said heating temperature for a total time determined to be sufficient for eliminating said voids, and thereafter said sheet encapsulated material is increased in temperature to the curing temperature or higher.

10. (Amended) The method as claimed in claim [1] 7, wherein the covering of said sheet encapsulating material is carried out by successively placing said sheet encapsulating material over said wafer from the end of said sheet encapsulating material so as to expel air.

11. (Amended) The method as claimed in claim [1] 7, wherein said bumps are formed in such a manner that the positions thereof as viewed from the main surface side

of said wafer and those of said electrode pads are rendered different from one another on a plane basis.

12. (Amended) The method as claimed in claim [1] 3, wherein said external terminals are formed after the formation of a wiring metal over said sheet encapsulating material in such a manner that the positions of said bumps as viewed from the main surface side of said wafer and those of said external terminals are different from one another on a plane basis.

14. (Amended) The method as claimed in claim [1] 7, wherein said sheet encapsulating material contains a curing agent for curing said thermosetting resin, in a state in which said curing agent is enclosed in a capsule broken at said curing temperature.

15. (Amended) The method as claimed in claim [1] 7, wherein said sheet encapsulating material contains an antifoaming agent for removing said voids contained in said sheet encapsulating material.